

## **REMARKS**

### **Status of the Claims**

Claims 5, 6, and 9-11 are now present in this application. Claims 5 and 9 are independent.

Claim 8 has been canceled, and claims 5 and 9 have been amended. Reconsideration of this application, as amended, is respectfully requested.

### **Rejections under 35 U.S.C. § 103**

Claims 5, 6, 9, and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuhara (US 6,535,316) in view of Miyamoto et al. (US 6,559,996), Conradi (US 2003/0156774), and Kikuchi et al. (US 6,850,713). Further, claims 8 and 11 stand rejected under § 103(a) as being unpatentable over Mizuhara, Miyamoto, Conradi, and Kikuchi and further in view of Vrazel (US 2003/0156774) and Ziemer et al., "Principles of Communication," 3<sup>rd</sup> Ed., Houghton Mifflin, 1990, pp. 480-82. These rejections are respectfully traversed.

Complete discussions of the Examiner's rejections are set forth in the Office Action, and are not being repeated here.

While not conceding the appropriateness of the Examiner's rejection, but merely to advance prosecution of the instant application, Applicants respectfully submit that independent claim 1 has been amended to recite a combination of elements in an optical transmitter including:

a first encoder that generates a differentially encoded signal..., the first encoder including a one-bit delay circuit, an exclusive OR circuit, and a differential circuit that is electrically connected to the exclusive OR circuit and outputs an inverted output signal and a non-inverted output signal, wherein the first encoder is configured so that an output signal of the exclusive OR circuit is input to the differential circuit, the inverted output signal of the differential circuit is input to the one-bit delay circuit, and an output signal of the one-bit delay circuit and the data signal is input to the exclusive OR circuit, the inverted output signal of the differential circuit being the positive phase differential signal, and the non-inverted output signal of the differential circuit being the reverse phase differential signal;

a second encoder to which a clock signal and the positive phase and the reverse phase differential signals are input, the second encoder being configured to generate an electric RZ (return-to-zero) differential signal as an RZ signal in an electric area from the differentially encoded signal, the electric RZ differential signal comprising a positive phase RZ signal and reverse phase RZ signal which are generated by the second encoder by synchronizing the positive phase and the reverse phase differential signals with the clock signal; and

a Mach-Zehnder interferometer type intensity modulator that generates an optical RZ-DPSK (differential phase shift keying) signal as an RZ signal in an optical area based on the electric RZ differential signal

(emphasis added).

The subject matter added by the amendments is supported in the original application, e.g., at page 9, line 30 to page 11, line 23; and Fig. 3.

Applicants respectfully submit that this combination of elements as set forth in independent claim 5, as amended, is not disclosed or made obvious by Mizuhara, Miyamoto, Conradi, and Kikuchi, when considered separately or in obvious combination. Particularly, none of these references teach or suggest the first encoder in the amended claim.

Mizuhara is relied upon as the primary reference in the Examiner's rejection. In page 2 of the Office Action, the Examiner acknowledges that Mizuhara does not disclose a differential encoder. Therefore, Mizuhara cannot be relied upon to teach or suggest the claimed first encoder. Furthermore, Applicants respectfully submit that Mizuhara also fails to disclose the claimed Mach-Zehnder interferometer type intensity modulator. Even though Mizuhara's optical modulator 305 is based on a Mach-Zehnder interferometer design, the output 311 of Mizuhara's optical modulator 305 is a "high-speed digital optical signal having NRZ (non-return-to-zero) properties" (col. 3, lines 55-56; emphasis added), not an RZ signal as claimed.

As to Miyamoto, the Examiner cites to this reference as teaching a differential encoder (see Office action at page 2). However, Miyamoto does not disclose either the claimed first encoder. For instance, Miyamoto fails to teach or suggest a differential encoder in which the inverted output signal of the differential circuit is input to the one-bit delay circuit, as required of the claimed first encoder. Instead, Figs. 11, 13, and 22 of Miyamoto show that the output of an exclusive-OR circuit is directly input to the one-bit delay circuit. Miyamoto also fails to disclose the second encoder. Even assuming *arguendo* that the combination of bandpass filters 2, 2' and drive circuits 3, 3' in Miyamoto could be considered an encoder to which positive phase and reverse phase differential signals are input, Miyamoto does not teach or suggest synchronizing such positive phase and reverse phase differential signals with a clock signal as claimed.

As to Conradi, the Examiner cites to this reference as teaching an NRZ-to-RZ converter comprising an AND gate and a clock signal (see Office Action at page 3). While Conradi

describes Fig. 5 as showing that “an optional NRZ to RZ converter logic block 600 is additionally inserted...to convert an NRZ signal 220 from the data source 22’ to the RZ signal 422” (paragraph 0036), this logic block 600 is shown as synchronizing a unipolar NRZ signal to a clock signal, not a differentially encoded signal with positive and reverse phases. Therefore, this embodiment in Conradi does not teach or suggest the claimed first encoder because it does not generate a differentially encoded signal comprising positive phase and reverse phase differential signals. Furthermore, this embodiment in Conradi does not teach or suggest the claimed second encoder because it does not synchronize both positive phase and reverse phase differential signals to the same clock signal as claimed.

As to Kikuchi, the Examiner cites to this reference to teach using the same clock signal to synchronize the signals of two RZ converters (see Office Action at page 3). However, similar to the other references, Kikuchi fails to disclose the first encoder as recited in amended claim 5. Particularly, there is no teaching or suggestion in Kikuchi of, nor any assertion by the Examiner that Kikuchi teaches or suggests, a first encoder including “a one-bit delay circuit, an exclusive OR circuit, and a differential circuit that is electrically connected to the exclusive OR circuit and outputs an inverted output signal and a non-inverted output signal, wherein the first encoder is configured so that an output signal of the exclusive OR circuit is input to the differential circuit, the inverted output signal of the differential circuit is input to the one-bit delay circuit, and an output signal of the one-bit delay circuit and the data signal is input to the exclusive OR circuit, the inverted output signal of the differential circuit being the positive phase differential signal, and the non-inverted output signal of the differential circuit being the reverse phase differential signal” as required by claim 5.

For reasons explained above, Mizuhara, Miyamoto, Conradi, and Kikuchi do not teach or suggest every claimed feature as recited in independent claim 5, particularly the first encoder, when considered separately or in obvious combination.

As to Vrazel and Ziemer, neither of these references remedy the deficiencies of Mizuhara, Miyamoto, Conradi, and Kikuchi as set forth above in connection with independent claim 5. Particularly, neither Vrazel nor Ziemer discloses the claimed first encoder because neither reference discloses an encoder that generates a differentially encoded signal from a data signal including a differential circuit that is electrically connected to the exclusive OR circuit and

outputs an inverted output signal and a non-inverted output signal. Thus, even if Vrazel and/or Ziemer were combined with the other aforementioned references, the combination of references would still fail to teach or suggest the combination of elements recited in independent claim 5.

Applicants respectfully submit that the combination of elements as set forth in independent claim 5, as amended, is not disclosed or made obvious by the prior art of record for the reasons explained above. Further, it is respectfully submitted that independent claim 9 has been amended *mutatis mutandis*, and thus is allowable over the prior art off record for similar reasons as claim 5. Further, claims 6, 10, and 11 depend from independent claims 5 and 9, and thus are allowable at least by virtue of their dependence from claims 5 and 9. Accordingly, reconsideration and withdrawal of these rejections are respectfully requested.

### **Conclusion**

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

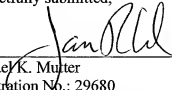
In view of the above amendment, Applicants believe the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Jason Rhodes (Registration Number 47,305) at (703) 208-4011 to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Director is hereby authorized in this, concurrent, and future replies to charge any fees required during the pendency of the above-identified application or credit any overpayment to Deposit Account No. 02-2448.

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Respectfully submitted,

for By  #47,305  
Michael K. Mutter  
Registration No.: 29680  
BIRCH, STEWART, KOLASCH & BIRCH, LLP  
8110 Gatehouse Road, Suite 100 East  
P.O. Box 747  
Falls Church, VA 22040-0747  
703-205-8000